A New Power W-Gated Trench MOSFET (WMOSFET) with High Switching Performance

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Abstract: **A new power Trench MOSFET with W-shaped gate structure (WMOSFET) that demonstrates a significant reduction in gate-drain charge Qgd, a low on-resistance, and good production process margin is reported. The gate is formed using a thicker oxide at the bottom of the trench that is self-aligned to the P-body / N-epi junction. Fabricated 35 V N-channel devices exhibit a Rdson * Qgd Figure of Merit of 12.5 mΩ.nC with V_{GS}=10V and V_{DD}=15V. Experimental data of devices fabricated using LOCOS and Sub Atmospheric CVD (SACVD) processes to form the thicker oxide layer along with simulation results are presented.**

INTRODUCTION

The trench-gated U-groove MOSFET or UMOSFET has become the device of choice for ultra-low on-resistance power MOSFETs in many power management applications. Advances in dc-dc converters require increasing the efficiency by minimizing both conduction and switching losses while operating the power MOSFET at ever increasing currents and frequencies. Such requirements drive further scaling in cell pitch and minimizing gate charge. The challenge in scaling conventional UMOSFET is that its structure suffers from an inherent high gate-drain or Miller capacitance C_{rss} as shown in Figure 1(a). Therefore, further increase in UMOSFET cell densities is accompanied by an increase in C_{rss} which degrades device switching performance. To address this problem, structures such as shown in Figure 1(b) have been proposed that feature a thicker gate oxide at the trench bottom [1-2]. However, such structures do not provide the potential optimum performance of minimum C_{rss}. Taking into consideration process variations in both trench and p-body junction depths a certain overlap between the thin gate oxide and drain region is required to allow the current to flow. Alternatively, lower C_{rss} can be achieved by reducing the trench width to deep submicron dimensions [3]. The latter approach can result in a lower current carrying capability due to the pinching of the P-body JFET.

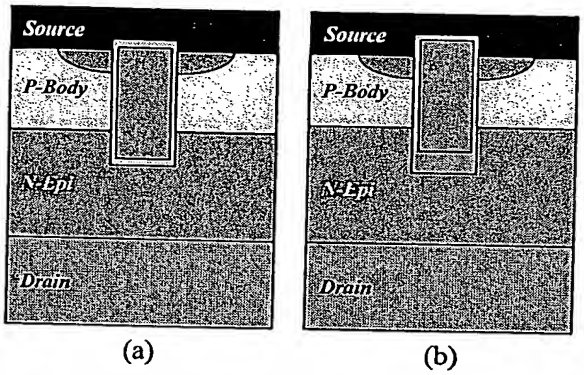

Figure 1. Schematic cross section of a) Conventional and b) Thick bottom oxide Trench MOSFETs.

W-GATED TRENCH MOSFET (WMOSFET)

The new structure [4] shown in Figure 2 utilizes a thin gate oxide along the vertical walls and a thicker oxide at bottom of the trench. The improvement over

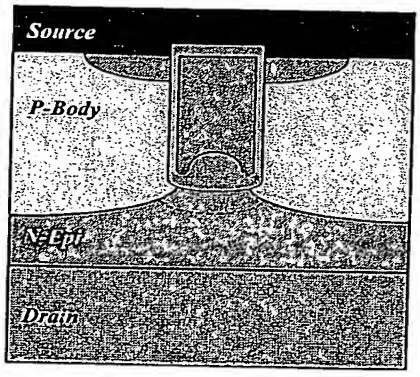

Figure 2. Schematic cross section of a W-Gated Trench MOSFET (WMOSFET).

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state of the art structures is achieved by shaping the gate such that the thicker gate oxide at the bottom of the trench is self-aligned to the P-body / N-epi junction with a gradual transition to a thinner oxide along the trench walls and corners which results in a W-shaped gate. A slightly deeper p-body junction than the trench depth results in a lower capacitance as the source drain voltage starts to increase. Such structure allows further increase in cell density, for lower specific on-resistance, without sacrificing switching performance.

FABRICATION PROCESS

Devices were fabricated using a PWM optimized Trench MOSFET process with various cell pitch, gate oxide thickness and trench depths. Standard Trench MOSFET core process was used with an additional module. The process flow included a deposited nitride layer after the trench etch and pad oxide growth. The nitride layer is then removed only from the trench bottom. Self-alignment is achieved with a lightly doped arsenic implant at the bottom of the trench, as seen in the simulated 2D doping profile of Figure 3. A thick bottom oxide layer in the range of 100 - 200 nm is then realized by either using a LOCOS or SACVD process.

The self–aligned arsenic implant minimizes the impact of the thicker oxide on on-resistance and provides a good process margin. Simulations show that this effect is further aided by the following effects: a) a slower lateral than vertical diffusion of the P-body region, b) P-body boron segregation and c) N-epi phosphorus pile-up at the oxide interface.

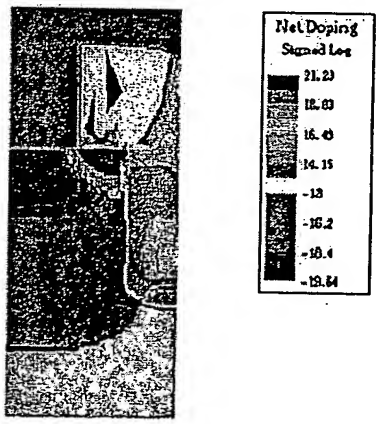

Figure 3: 2D doping profile in a W-gated Trench MOSFET.

The LOCOS process is easily implemented and provides a smooth transition between the thin and thick oxide layers as can be seen in Figure 4. A SEM cross-sections of W-gated Trench MOSFET (WMOSFET) with a thin oxide of 50nm and a thick bottom oxide of 150 nm. The potential stress issue at the bird's beak is minimized by process and device design.

The alternative SACVD process utilizes the high selectivity deposition rate of ozone-activated TEOS Sub-Atmospheric CVD on the exposed N-epi layer at the bottom of the trench. This is achieved by using the nitride film as a mask on the trench sidewalls. The SACVD deposition rate difference on Si vs. nitride substrate is modest (~ 2) for a planar surface, nevertheless the selectivity is much more significant (>50) when a vertical plane is encountered.

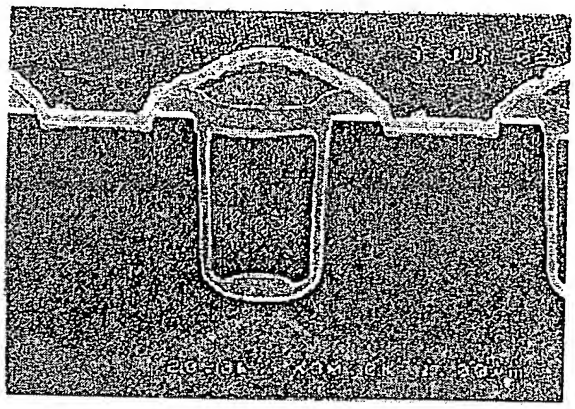

Figure 4: SEM cross section of a W-Gated Trench MOSFET formed using LOCOS process.

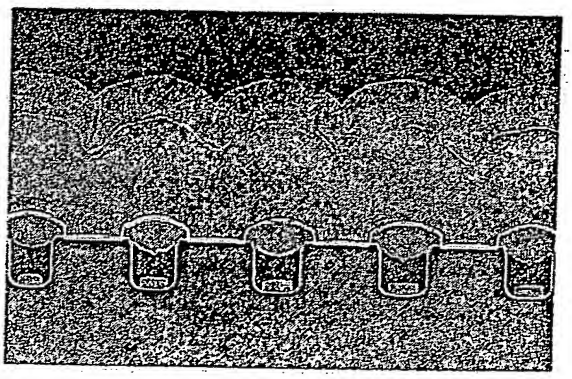

Figure 5: SEM cross section of a W-Gated Trench MOSFET formed using SACVD process.

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Furthermore, the film deposited on nitride surface is more porous and consequently has a higher etch rate. By inherently having both differential deposition and differential etch advantages, this approach yields a better capability of retaining the thick bottom oxide. However in order to get better film quality, an additional high-temperature anneal is required for SACVD film. Since this approach is a deposition process, no silicon formation consumption is involved as compared to the LOCOS approach and the stress created at bird's beak is avoided. It should also be noted that the thick bottom oxide formed by SACVD has a steeper edge by the nature of the deposition process as shown in Figure 5.

RESULTS AND DISCUSSION

W-gated MOSFET structures were optimized for dc-dc converter applications. Fabricated devices using different cell pitches ranging from 4.2μm to 2.4μm have breakdown voltage of 35 Volts. The devices were characterized and their performance was compared with conventional Trench MOSFETs fabricated using the same layout and core process.

The impact of the shape of the gate oxide on both breakdown voltage and on-state characteristics was investigated. A reduction in the electric field at the thin-thick oxide transition (bird's beak) is achieved by rounding the trench corners and properly designing the p-body junction to shield the corner region in addition to oxide growth process optimization. This is evident in the simulation results of the potential contours in the off-state with V_{GS}=0V and V_{DS}=35V as shown in Figure 6. Simulation results of conventional and WMOSFET agree with measured data which show no reduction in breakdown voltage.

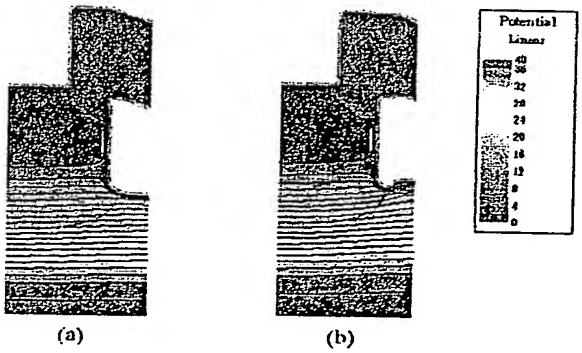

Figure 6: Equipotential contours in the off-state with Vds=35V for a) Conventional and b) W-gated Trench MOSFET (WMOSFET).

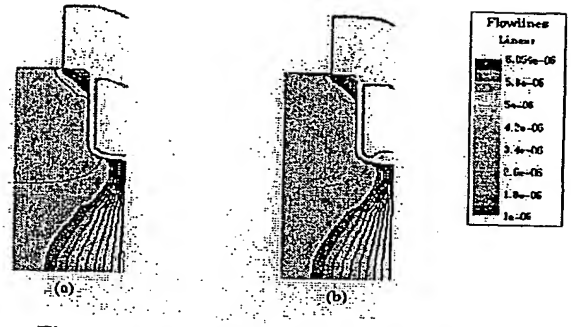

Figure 7: Current flowlines for VGS=5V in a) Conventional and b) W-gated Trench MOSFET.

In the on-state with V_{GS}=5V current spread at the bottom of the trench does not suffer from the JFET pinching effect as seen in Figure 7. However, an increase in the on-resistance of about 5% at Vgs=5V is predicted for a device with cell pitch of 2.4 μm and thin and bottom gate oxides of 50nm and 180nm respectively. This is due to a higher resistance of the accumulation layer at the trench bottom. Measured specific on-resistance of a WMOSFET with 2.4 μm cell pitch is 22 $m\Omega.mm^2$

A significant reduction in Crss of a WMOSFET compared to a conventional device is achieved as shown in Figure 8. For an optimized WMOSFET with thin and bottom oxide thickness of 50nm and 180 nm respectively, Crss at V_{DS} = 0V / 30V drops to 207 pF / 89 pF compared to 762 pF / 163 pF of a conventional device having the same active area and cell pitch.

The measured gate-drain charge Qgd with V_{DD}=15V was reduced to 1.6 nC, as shown in Figure 9. This corresponds to a Rdson*Qgd Figure of Merit of 12.5 mΩ.nC, with V_{GS}=10V, a factor of 2.5 improvement.

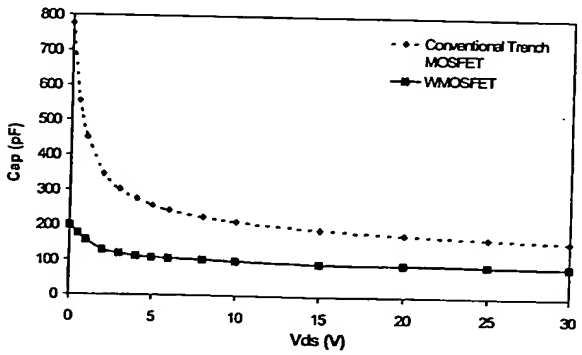

Figure 8: Measured Gate-Drain Capacitance Crss of a WMOSFET and a conventional Trench MOSFET.

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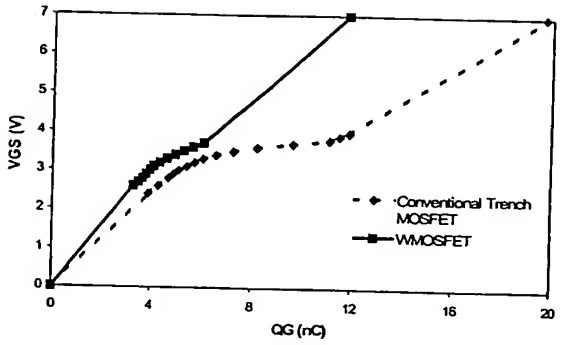

Figure 9: Measured Gate Charge of a W-Gated WMOSFET and a conventional Trench MOSFET.

Using different gate oxide thickness provides an extra degree of freedom in optimizing WMOSFEETs. The choice of thin and bottom gate oxide thickness values provides flexibility for a better specific on-resistance gate charge trade-off. Therefore, WMOSFET can be optimized for use in dc-dc converters as both a control and/or a synchronous switch.

As a control switch the WMOSFET has a low Figure of Merit Rdson*Qgd. The device can also be optimized for use as a synchronous switch. In addition to the low specific on-resistance, the device exhibits a low Qgd/Qgs ratio. This is important to minimize power loss due to shoot through. The measured Qgd/Qgs ratio of a conventional Trench MOSFET was reduced from 0.8 to 0.53 for a WMOSFET. Figure 10 shows the same effect as an improvement in C_{rss} to the input capacitance C_{iss} ratio for a WMOSFET with thin and bottom gate oxide thickness of 30nm and 1500nm respectively. This improvement can be utilized to optimize other important device parameters. For example, for the same switching power loss a lower

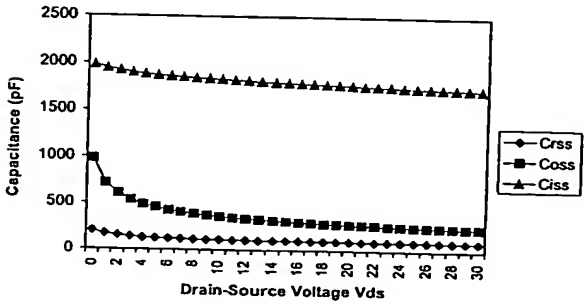

Figure 10: Input, output and transfer capacitance (Ciss, Coss and Crss) vs. drain voltage for a 30nm and 150nm gate oxide WMOSFET.

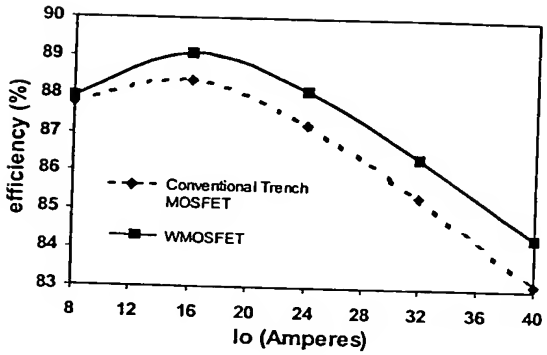

Figure 11. Measured efficiency vs. output current for a PWM switch-mode two-phase DC-DC Buck converter with 20V IN and 1.5V OUT.

threshold voltage can be used which results in reduced conduction losses.

The efficiency versus output current of a PWM switch-mode, synchronous, two phase, dc-dc buck converter with 20V Vin and 1.5 Vout using WMOSFETs as a control (high side) switch is shown in Figure 11. At a switching frequency of 300KHz 1.5% increase in efficiency is achieved over conventional MOSFETs.

CONCLUSION

A new power Trench MOSFET with W-shaped gate structure (WMOSFET) was presented. Devices with 35V breakdown voltage exhibit a low Rdson*Qgd figure of 12.5 mΩ.nC and a good production process margin. The gate is formed using a thicker oxide at the bottom of the trench that is self-aligned to the P-body / N-epi junction. Experimental data of devices fabricated using LOCOS and Sub Atmospheric CVD (SACVD) processes to form the thicker oxide layer at the bottom of the trench along were presented.

ACKNOWLEDGEMENT

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